UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,990	03/07/2005	Shridhar Mubaraq Mishra	1890-0213	6999

50255 7590 11/27/2007

MAGINOT, MOOR & BECK
111 MONUMENT CIRCLE, SUITE 3000
BANK ONE CENTER/TOWER
INDIANAPOLIS, IN 46204

EXAMINER	
RUTKOWSKI, JEFFREY M	
ART UNIT	**PAPER NUMBER**
2619	

MAIL DATE	DELIVERY MODE
11/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,990	MISHRA ET AL.	
	Examiner	Art Unit	
	Jeffrey M. Rutkowski	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/13/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-7 have been cancelled.

Claim Objections

1. **Claims 8-27** are objected to because of the following informalities: the claims contain undefined acronyms such as GE, FE and MAC. The examiner has interpreted the acronyms to mean Gigabit Ethernet, Fast Ethernet and Media Access Controller, respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 8-27** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims recite an ingress/egress port with a plurality of Media Access Control (MAC) interfaces. It is unclear as to whether or not the port terminates a single line or multiple lines as suggested by the partitioning of pins **[Specification, page 3 lines 15-20]**.

4. For **claim 19**, the use of the variable 'n' renders the claim indefinite because 'n' is not defined.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 8-11, 16-19 and 24-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadambi et al. (US Pat 6,104,696) in view of Moran et al. (US Pg Pub 2002/0071398), hereinafter referred to as Moran

8. For **claims 8, 17-18 and 24**, Kadambi teaches a switch on a single silicon chip **[figure 1]**. The switch includes Ethernet Port Interface Controllers (EPIC) and Gigabit Port Interface Controllers (GPIC) **[col. 4 lines 55-60 and figure 2]** (a plurality of MAC interfaces, each MAC interface is capable of receiving/transmitting FE packets, at least one of the MAC interfaces further being configurable to receive/transmit GE packets).

9. Kadambi teaches the EPIC and GPIC controllers send and receive information (FE and GE packets) to and from a Common Buffer Memory Pool (CBP). Kadambi does not teach the use of separate send and receive modules. Moran teaches the separate send and receive module limitation absent from the teachings of Kadambi by disclosing an architecture where a Media Access Controller (MAC) interacts with separate receive **30** and transmit **29** storage modules **[figure 2]** (receive and transmit modules which are configurable respectively to receive both GE

and FE packets from, and transmit GE and FE packets to, the interfaces). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use separate send and receive modules in Kambadi's invention to allow for a more efficient way to locate buffered frames by not having to search one large pool to locate a particular packet.

10. For **claims 9, 26 and 27**, which depend from **claims 8, 25 and 24 respectively**, Kadambi teaches controllers that provide only one type of service, either FE or GE services **[figure 2]** (other MAC interfaces only being adapted to receive/transmit FE packets). Kadambi does not teach a controller that will negotiate between FE and GE. Moran teaches the FE/GE negotiation absent from the teachings of Kadambi by disclosing Ethernet MAC controllers capable of negotiating 10/100/1000 Mbps transmission rates **[0019]** (wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use one of Moran's controllers in Kadambi's invention to provide a port that can be used as a high speed port (GE) or as a backup for other low speed ports (FE).

11. For **claims 10 and 11**, which depend from **claims 9 and 8 respectively**, Kadambi teaches each EPIC and GPIC contain ingress **14** and egress **16** sub-modules **[col. 10 line 65 to col. 11 line 10 and figure 8]** Also included in the EPIC and GPIC controllers is an input First In First Out (FIFO) memory that stores packets as they are received before the packet is sent to an internal memory (receive module) **[col. 16 lines 5-15 and figure 14]** (wherein which each MAC interface is associated with a buffer configured to store packets as they are received, the receive module being arranged to receive packets from the buffers sequentially, whereby the receive

module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously).

12. For **claim 16**, which depends from **claim 8**, Kadambi teaches any number of FE and GE ports can be provided **[col. 4 lines 40-45]** (wherein the plurality of MAC interfaces consists of 8 MAC interfaces).

13. For **claim 19**, which depends from **claim 18**, Kadambi teaches any number of FE and GE ports can be provided **[col. 4 lines 40-45]** (wherein the ingress/egress port and the other ingress/egress ports total eight ingress/egress ports).

14. Kadambi teaches controllers that provide either FE or GE services **[figure 2]**. Kadambi does not teach a controller that will negotiate between FE and GE. Moran teaches the FE/GE negotiation absent from the teachings of Kadambi by disclosing Ethernet MAC controllers capable of negotiating 10/100/1000 Mbps transmission rates **[0019]** (each ingress/egress port being switchable between two modes, a first mode operating as one GE port and a second mode operating as eight FE ports, and wherein the switch can operate as n GE ports and 8(8-n) FE ports). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use one of Moran's controllers in Kadambi's invention to provide a port that can be used as a high speed port or as a backup for other low speed ports.

15. For **claim 25**, which depends from **claim 24**, Kadambi does not teach a controller that will negotiate between FE and GE. Moran teaches the FE/GE negotiation absent from the teachings of Kadambi by disclosing Ethernet MAC controllers capable of auto-negotiating 10/100/1000 Mbps transmission rates **[0019]** (further comprising providing a control signal to the ingress/output port to determine whether the MAC interfaces operate as FE interfaces or

whether the at least one interface operates as a GE interface). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use one of Moran's controllers in Kadambi's invention to provide a port that can be used as a high speed port or as a backup for other low speed ports.

16. **Claims 12-15, 20-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadambi in view of Moran as applied to **claim 8** above, and further in view of Gentry, Jr. (US Pat 6,356,951), hereinafter referred to as Gentry.

17. For **claims 12 and 20**, which depend from **claims 8 and 17 respectively**, the combination of Kadambi and Moran, as discussed in the rejection of **claim 8**, discloses a receive module that stores packet data (wherein the receive module further includes a memory configured to store packet data).

18. The combination of Kadambi and Moran do not teach the use of a receiver that interfaces with a parser. Gentry teaches the receiver interfacing with a parser limitation absent from the teachings of Kadambi and Moran by disclosing an input port processing module **104** interfaces with a header parser **106 [figure 1A]**. The header parser **106** parses only the header (descriptor) portion of the packets **[col. 7 lines 50-55]** (a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module). It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a receiver interface in Kadambi's invention to identify related packets **[Gentry, col. 7 line 53]**.

19. For **claims 13, 15, 21, 23**, which depend from **claims 12, 13, 20 and 21 respectively**, the combination of Kadambi and Moran, as discussed in the rejection of **claim 8**, disclose a CBP

used as a receive module (claim 13: wherein the receive module further comprises a set of buffers configured to receive packets from at least one of the MAC interfaces).

20. The combination of Kadambi and Moran do not disclose a receiver interface fetching packet data from the CBP (set of buffers). Gentry teaches the receiver interface fetching data limitation absent from the teachings of the combination of Kadambi and Moran by disclosing the header parser **106** copies header information (descriptor) from input port processing module **104** into a header memory **302 [col. 17 lines 8-9 and figure 3]** (claim 13: wherein the receiver interface is further operable to fetch packet data from the set of buffers and store the packet data in the memory; claim 15: wherein the receiver interface is further operable to store the descriptor associated with the packet data in the memory). It would have been obvious to a person of ordinary skill at the time of the invention to fetch and store information from the receive module and place it in a header memory in Kadambi's invention to minimize the number of read requests between the different modules.

21. For **claims 14 and 22**, which depend from **claims 13 and 21 respectively**, the combination of Kadambi and Moran, as discussed in the rejection of **claim 8**, disclose a CBP used as a receive module. The combination of Kadambi and Moran do not disclose the buffers in the CBP are FIFO buffers. Gentry teaches the FIFO buffer limitation absent from the teachings of the combination of Kadambi and Moran by disclosing the input processing module **104** stores packet information in a FIFO packet queue **116 [col. 51 lines 58-60 and figure 1A]** (wherein each buffer of the set of buffers comprises a first-in-first-out buffer). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a set of FIFO buffers in the CBP to provide fairness when processing packets.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey M. Rutkowski whose telephone number is (571) 270-1215. The examiner can normally be reached on Monday - Friday 7:30-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey M Rutkowski
Patent Examiner
11/21/2007

JMR

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600